Design Consideration with AP3502/3

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1. Introduction

The AP3502/3 are current-mode step-down DC-DC converters, capable of driving a 2A/3A load with high efficiency, excellent line and load regulation. The AP3502/3 integrate cycle-by-cycle current limit protection, programmable soft-start, short circuit protection and over temperature protection, which can notably increase the system reliability.

The AP3502/3 are synchronous step-down converters with internal power MOSFETs. Turn on/off M1 and M2 alternately to chop the input voltage. The current sense signal is compared with the EA output signal to regulate the output voltage and adjust the MOSFETs' duty cycle. The AP3502/3 are also high reliability ICs with integrated OCP, OVP, OTP, UVLO circuit. For more information please refer to the functional block diagram (Figure 1).

2. General Description

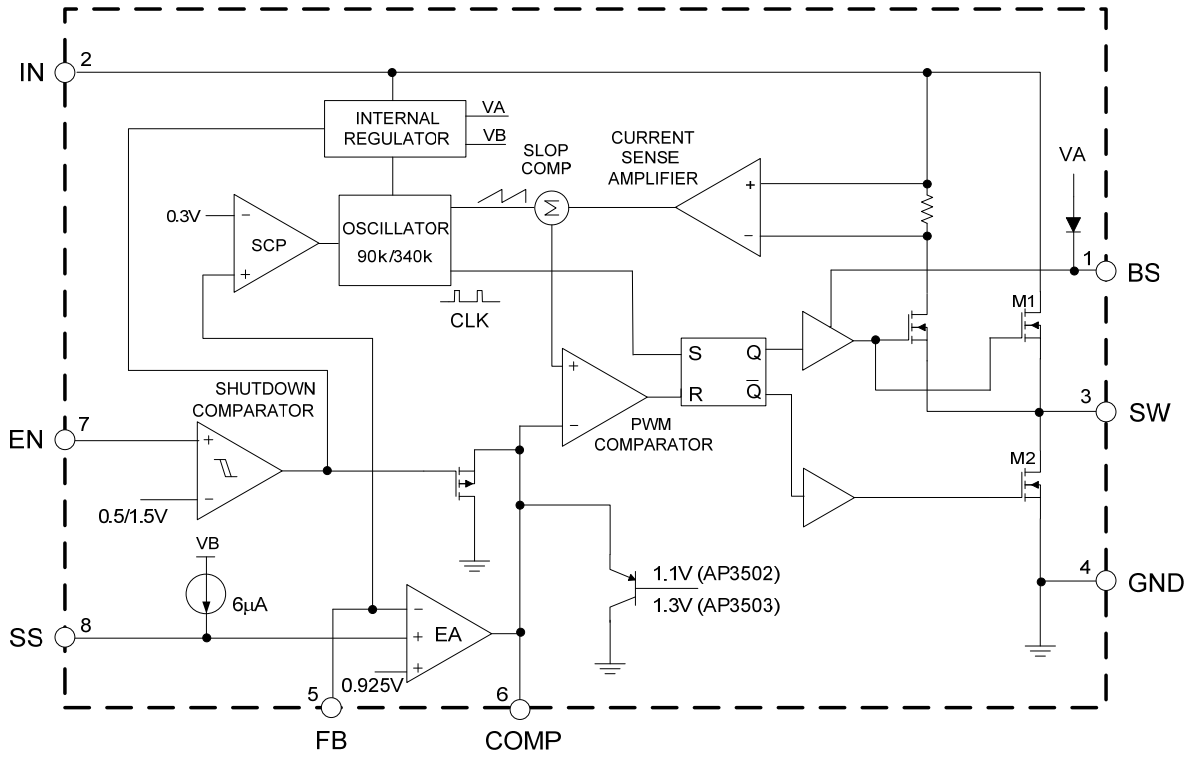

Figure 1. Functional Block Diagram of AP3502/3

2.1 Programmable Soft-start

The soft-start time of the AP3502/3 is fully user programmable by selecting different C_{SS} value. The C_{SS} is charged by a 6μA current source, generating a ramp signal fed into non-inverting input of the error amplifier. And this ramp signal will regulate the voltage on COMP pin when starting the system, thus realizing soft-start. The capacitor value required for a given soft-start ramp time can be expressed as:

$$C_{SS} = t_{SS} \times \frac{6\mu A}{V_{FB}}$$

Where C_{SS} is the required capacitor between SS pin and GND, t_{SS} is the desired soft-start time and V_{FB} is the feedback voltage.

2.2 Over Current Protection

The AP3502/3 have internal over current protection function to protect themselves from catastrophic failure. The AP3502/3 can monitor the drain-to-source current of M1. The peak current-limit threshold is internally set at 3.5/5.6A. When the inductor current is higher than the current limit threshold, OCP function will be triggered, forcing M1 to turn off, and this will last until the next switching cycle.

2.3 Short Circuit Protection

The V_{FB} is proportional to V_{OUT}. When the output terminal is shorted and V_{FB} is below 0.3V, the operating frequency will reduce to 90kHz for system protection. The AP3502/3 will restart once released from OCP condition.

2.4 Over Voltage Protection

The AP3502/3 have internal OVP circuits. When V_{OUT} is higher than the OVP threshold, the power switching will be turned off. The AP3502/3 will restart once released from OCP condition.

2.5 Over Temperature Protection

The OTP circuitry is provided to protect the IC if the maximum junction temperature is exceeded. When the junction temperature exceeds 160ºC, it will shut down the internal control circuit, M1 and M2. The AP3502/3 will restart automatically under the control of soft-start circuit when the junction temperature decreases to 130ºC/140ºC.

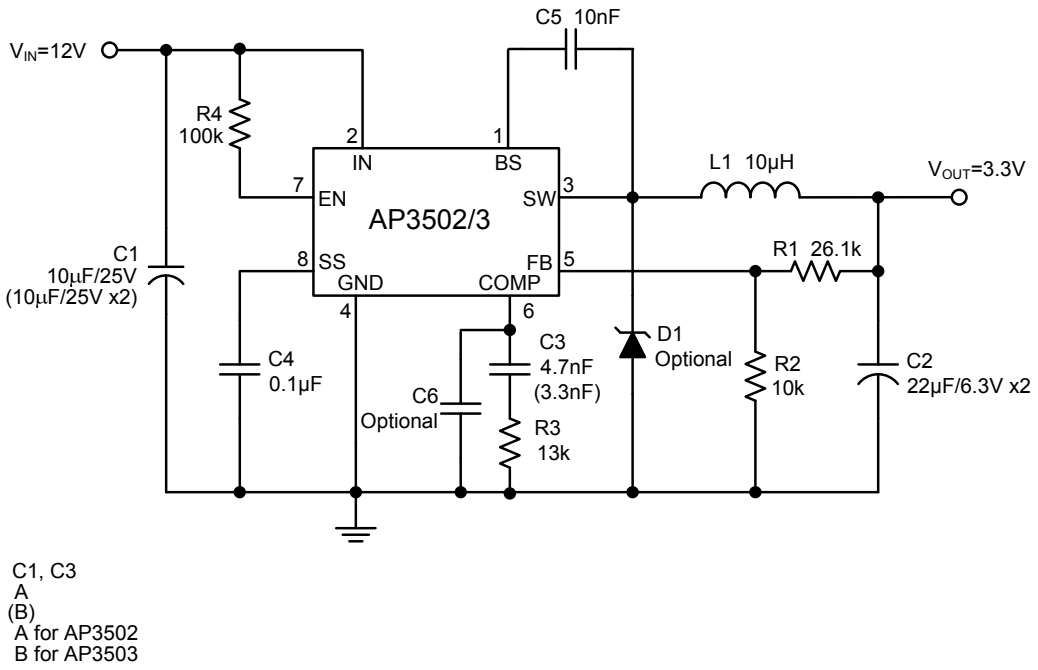

Figure 2. Typical Application of AP3502/3

3. Application Information

Typical application circuit is shown in the Figure 2, and for the circuit parameters setting please refer to the following descriptions.

3.1 Output Voltage Setting

The output voltage can be set using a voltage divider from the output to FB pin. V_{OUT} is divided by the voltage divider as below:

$$V_{FB} = V_{OUT} \times \left(\frac{R2}{R1 + R2} \right)$$

Where V_{FB} is the feedback voltage, and V_{FB}=0.925V. Thus, V_{OUT} can be expressed as:

$$V_{OUT} = 0.925 \times \left(\frac{R1 + R2}{R2} \right)$$

First, fix R2 based on the recommended value, 10kΩ. Then, R1 can be expressed as:

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.925} - 1 \right)$$

3.2 Inductor Setting

The inductor is used to supply smooth current to output when driven by a switching voltage. Its value relies on the operating frequency, load current, ripple current, and duty cycle.

A higher-value inductor can decrease the ripple current and output ripple voltage, however usually with larger physical size. So some compromise needs to be made when selecting the inductor. The peak-to-peak inductor ripple current is 26% of the maximum output current when operating in continuous mode (In most applications, a good compromise is from 20% to 30% of the maximum load current of the converter), and the inductor L1 can be selected according to:

$$L1 = V_{OUT} \times \frac{V_{IN} - V_{OUT}}{f_{SW} \times V_{IN} \times I_{OUT} \times 26\%}$$

Where V_{IN} is the input voltage, I_{OUT} is the output current, and f_{SW} is the oscillator frequency.

Another important parameter for the inductor is the current rating. After fixing the inductor value, the peak inductor current can be expressed as:

$$I_{PEAK} = I_{OUT} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{SW} \times L1}$$

Where I_{PEAK} is the peak inductor current.

The current rating of the selected inductor should be ensured to be 1.5 times of the peak inductor current.

3.3 Input Capacitor Setting

A high-quality input capacitor with big value is needed to filter noise at input voltage source and limit the input ripple voltage while supplying most of the switch current during ON time. For input capacitor selection, a ceramic capacitor is highly recommended due to its low impedance and small size. However, tantalum or low electrolytic capacitor is also sufficed.

There are two important parameters of the input capacitor: the voltage rating and RMS current rating. The voltage rating should be at least 1.25 times greater than the maximum input voltage, and the RMS current of input capacitor can be expressed as:

$$I_{CIN\_RMS} = I_{OUT}(MAX) \times \sqrt{\frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

Where I_{CIN_RMS} is the RMS current of input capacitor.

As indicated by the RMS current equation above, I_{CIN_RMS} reaches the highest level at the duty cycle of 50%. So the RMS current of input capacitor should be greater than half of the output current under this worst case. For reliable operation and best performance, ceramic capacitors are preferred for input capacitor because of their low ESR and high ripple current rating. And X5R or X7R type dielectric ceramic capacitors are preferred due to their better temperature and voltage characteristics. Additionally, when selecting ceramic capacitor, make sure its capacitance is big enough to provide sufficient charge to prevent excessive voltage ripple at input. The input ripple voltage can be approximately expressed as below:

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \times \frac{V_{OUT}}{V_{IN}}$$

Where ΔV_{IN} is the input ripple voltage.

3.4 Output Capacitor Setting

The output capacitor can be selected based upon the desired output ripple and transient response. The output voltage ripple depends directly on the ripple current and is affected by two parameters of the output capacitor: total capacitance and the Equivalent Series Resistance (ESR). The output ripple voltage can be expressed as:

$$\Delta V_O = \Delta I_L \times \left[R_{ESR} + \left(\frac{1}{8 \times C_{OUT} \times f_{SW}} \right) \right]$$

Where ΔV_O is the output ripple voltage, and R_{ESR} is ESR of output capacitor.

For lower output ripple voltage across the entire operating temperature range, X5R or X7R ceramic dielectric capacitor, or other low ESR tantalum capacitor or aluminum electrolytic capacitor are recommended.

The output capacitor selection will also affect the output drop voltage during load transient. The output drop voltage during load transient is dependent on many factors. However, an approximation of the transient drop ignoring loop bandwidth can be expressed as:

$$V_{DROP} = \Delta I_{TRAN} \times R_{ESR} + \frac{L \times \Delta I_{TRAN}^{\ 2}}{C_{OUT} \times (V_{IN} - V_{OUT})}$$

Where ΔI_{TRAN} is the output transient load current step, and V_{DROP} is the output voltage drop (ignoring loop bandwidth).

Both the voltage rating and RMS current rating of the capacitor needs to be carefully examined when designing a specific output ripple or transient drop. The output capacitor voltage rating should be greater than 1.5 times of the maximum output voltage. In the buck converter, output capacitor current is continuous. The RMS current is decided by the peak-to-peak inductor ripple current. It can be expressed as:

$$I_{COUT\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

Where I_{COUT_RMS} is the RMS current of output capacitor

3.5 Loop Compensation

The AP3502/3 employs current-mode control to achieve easy compensation and fast dynamic response. Optimal loop compensation depends on the output capacitor, inductor, load, compensation network and also the device itself. For a stable system, the values for the compensation network is shown in Table 1 and Table 2.

V_{IN}/V_{OUT} (V)	R1 (kΩ)	C3 (nF)	R3 (kΩ)
12/1.2	3	4.7	7.5
12/1.8	9.53	6.8	15
12/2.5	16.9	5.6	13
12/3.3	26.1	4.7	13
12/5	44.1	3.3	13

Table 1. AP3502 Compensation Value R-C Combination

V_{IN}/V_{OUT} (V)	R1 (kΩ)	C3 (nF)	R3 (kΩ)
12/1.2	3	6.8	7.5
12/1.8	9.53	6.8	10
12/2.5	16.9	5.6	10
12/3.3	26.1	3.3	13
12/5	44.1	2.2	13

Table 2. AP3503 Compensation Value R-C Combination

If the V_{IN}/V_{OUT} value of desired solution are not found from the table above, the loop transfer function should be analyzed to optimize the loop compensation. The overall loop transfer function is the product of the power stage and the feedback network transfer function. The power stage transfer function is dictated by the modulator, the output LC filter and load. The feedback transfer function is dictated by the error amplifier gain, external compensation network and feedback resistor ratio. The purpose of loop compensation is to shape the loop transfer function in order to meet the desired loop gain. The crossover frequency should be set firstly. Because lower crossover frequency may result in slower line/load transient responses, while higher crossover frequency may result in system instability. A good compromise is to set the crossover frequency below 10% of the switching frequency. The crossover frequency (f_C) can be expressed as below:

$$f_C = \left(\frac{G_{EA} \times G_{CS} \times R3}{2\pi \times C_{OUT}} \times \frac{V_{FB}}{V_{OUT}} \right) < 0.1 \times f_{SW}$$

Where f_C is the crossover frequency, G_{EA} is the error

amplifier voltage gain, G_{CS} is the current sense trans-conductance. And the desired crossover frequency can be set via compensation resister R3.

For sufficient phase margin, the loop gain slope should be -20db/decade at the cross frequency. To suffice this requirement, the output filter pole (f_{P_OUT}), which is product by output capacitor and the load resister, should be cancelled by the zero point of error amplifier (f_{Z_EA}) due to the compensation capacitor (C3) and the output resistor of the error amplifier. They can be expressed as:

$$f_{P\_OUT} = \left(\frac{1}{2\pi \times C_{OUT} \times R_{OUT}} \right)$$

$$f_{Z\_EA} = \left(\frac{1}{2\pi \times C3 \times R3} \right)$$

Where, f_{P_OUT} is the output filter pole and f_{Z_EA} is the zero point of error amplifier.

In general, we can set f_{Z_EA} below one-forth of the f_C. So the value of C3 is determined by the following equation:

$$C3 > \frac{4}{2\pi \times R3 \times f_C}$$

R3 and C3 should be set appropriately to make sure the system work at the desired transient voltage drop and setting time. If the output capacitor has a large capacitance and/or a high ESR value, the zero point resulting from the output capacitor as well as its ESR should be considered. In this case, the additional capacitor (C6) should be placed between the COMP pin and GND. And, C6 can add a pole to the circuit, thus increasing the mid-frequency width of the control circuit.

$$f_{Z\_ESR} = \left(\frac{1}{2\pi \times C_{OUT} \times R_{ESR}} \right)$$

Where f_{Z_ESR} is the zero point of output filter. If needed, the value of C6 can be expressed as:

$$C6 = \frac{C_{OUT} \times R_{ESR}}{R3}$$

3.6 Bootstrap Capacitor

The bootstrap capacitor provided is used to drive the power switch's gate above the supply voltage. The bootstrap capacitor is supplied by an internal 5V supply and placed between SW pin and BS pin to form a floating supply across the power switch driver. So the bootstrap capacitor should be a good quality and high-frequency ceramic capacitor. For best performance, the bootstrap capacitor should be X5R and X7R ceramic capacitor, and is recommended to be 10nF.

4. PCB Layout Guidance

PCB layout is an important part for DC-DC converter design. Poor PCB layout may reduce the converter performance and disrupt its surrounding circuitry due to EMI. A good PCB layout should follow guidance below:

4.1 Power Path Length

The power path of AP3502/3 includes an input capacitor, output inductor and output capacitor. Place them on the same side of PCB and connect them with thick traces or copper planes on the same layer. The power components must be kept together closely. The longer the paths, the more they act as antennas, radiating unwanted EMI.

4.2 Coupling Noise

The external control components should be place as close to the IC as possible.

4.3 Feedback Net

Special attention should be paid to the route of the feedback wring. The feedback trace should be routed far away from the inductor and noisy power traces. Try to minimize trace length to the FB pin and connect feedback network behind the output capacitors.

4.4 Via Hole

Be careful to the via hole. Via hole will result in high resistance and inductance to the power path. If heavy switching current must be routed through via holes and/or internal planes, use multiple parallel via holes to reduce their resistance and inductance.

Typical examples of AP3502/3 PCB layer are shown in Figure 3 and Figure 4.

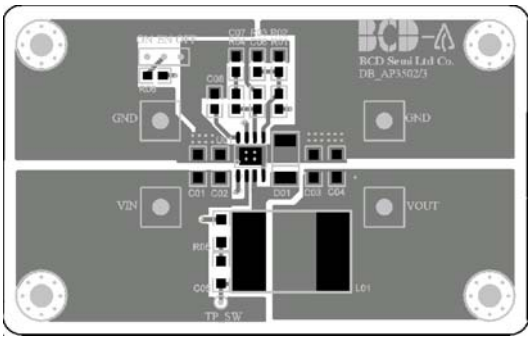

Figure 3. Top Layer

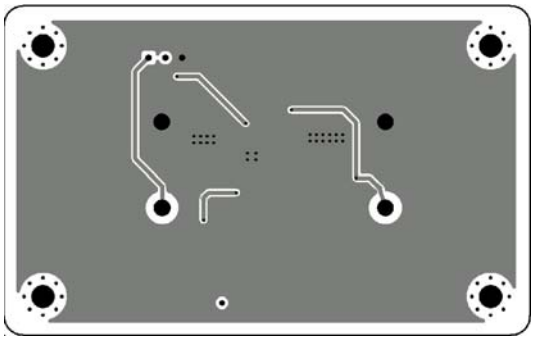

Figure 4. Bottom Layer